Docket No.: 209412US-2

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
HIDETOSHI EMA ET AL	: ATTN: APPLICATION DIVISION
SERIAL NO: 09/873,256	:
FILED: JUNE 5, 2001	:

FOR: IMAGE FORMING APPARATUS FOR CONTROLLING IMAGE WRITING BY ADJUSTING IMAGE CLOCK

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Prior to examination on the merits, please amend this application as follows:

IN THE CLAIMS

Please renumber and amend Claims 35-43 at pages 95-99 in this specification to read as follows. A marked-up copy of these claims is attached.

36. (Amended) An image forming apparatus comprising:

an optical scanning unit which scans a plurality of light fluxes on a medium to be scanned by deflecting the light fluxes by a deflector, the light fluxes being synchronous with an output pixel clock and being modulated in accordance with image data of a respective one of a plurality of lines; and

a clock phase control circuit which controls a phase of said output pixel clock for each of a plurality of deflecting surfaces of said deflector so as to correct a fluctuation in a scanning length corresponding to the plurality of deflecting surfaces.

37. (Amended) The image forming apparatus as claimed in claim 36, wherein said clock phase control circuit comprises:

a high-frequency clock generator;

a first frequency divider which generates said output pixel clock by dividing an output of said high-frequency clock generator, the first frequency divider having a circuit which can change a phase of said output pixel clock;

a phase change circuit which changes a phase of said first frequency divider; and

a second frequency divider which generates an internal clock by dividing an output of said high-frequency clock generator, the second frequency divider having a circuit which can change a phase of said internal clock.

38. (Amended) The image forming apparatus as claimed in claim 26, wherein said high-frequency clock generator is constituted by a PLL circuit comprising: a voltage controlled oscillator circuit; a programmable counter which divides an output of said voltage controlled oscillator circuit; and a phase comparator circuit which compares phases of an output of said programmable counter and a reference frequency, wherein said first frequency divider generates said output pixel clock by dividing an output of said voltage controlled oscillator circuit and a phase of said output pixel clock is synchronized with a phase synchronous signal.

39. (Amended) The image forming apparatus as claimed in claim 38, further comprising a modulation pattern generating circuit which generates a modulation pattern by

which an optimum exposure energy is obtained based on the image data in synchronization with said output pixel clock.

40. (Amended) The image forming apparatus as claimed in claim 39, wherein said modulation pattern generating circuit can change a phase of the output pixel clock for each of a plurality of lines.

41. (Amended) The image forming apparatus as claimed in claim 40, wherein said first frequency divider, said phase change circuit, said PLL circuit and said modulation pattern generating circuit are formed in a single integrated circuit.

42. (Amended) The image forming apparatus as claimed in claim 41, wherein said integrated circuit further comprises a semiconductor laser modulation drive circuit.

43. (Amended) An image forming apparatus comprising:

an optical scanning unit which scans a plurality of light fluxes on a medium to be scanned by deflecting the light fluxes by a deflector, the light fluxes being synchronous with an output pixel clock and being modulated in accordance with image data of a respective one of a plurality of lines; and

clock phase control means for controlling a phase of said output pixel clock for each of a plurality of deflecting surfaces of said deflector so as to correct a fluctuation in a scanning length corresponding to the plurality of deflecting surfaces.

44. (Amended) The image forming apparatus as claimed in claim 43, wherein said clock phase control means comprises:

high-frequency clock generator means;

first frequency dividing means for generating said output pixel clock by dividing an output of said high-frequency clock generator means, the first frequency dividing means having means for changing a phase of said output pixel clock;

phase change means for changing a phase of said first frequency dividing means; and

second frequency dividing means for generating an internal clock by dividing an output of said high-frequency clock generator means, the second frequency dividing means having means for changing a phase of said internal clock.

REMARKS

Favorable consideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-44 are pending in the present application with Claims 35-43 at pages 95-99 in the specification being renumbered and amended by the present Preliminary Amendment.

Applicants note there were two original Claims 35 in the English translation (see pages 94 and 95). Accordingly, this Preliminary Amendment appropriately renumbers the claims. The dependency of the claims has also been corrected. No new matter has been added.

Consequently, an action on the merits is earnestly solicited.

Respectfully submitted,

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IN THE CLAIMS

[35] 36. (Amended) An image forming apparatus comprising:

an optical scanning unit which scans a plurality of light fluxes on a medium to be scanned by deflecting the light fluxes by a deflector, the light fluxes being synchronous with an output pixel clock and being modulated in accordance with image data of a respective one of a plurality of lines; and

a clock phase control circuit which controls a phase of said output pixel clock for each of a plurality of deflecting surfaces of said deflector so as to correct a fluctuation in a scanning length corresponding to the plurality of deflecting surfaces.

[36]37. (Amended) The image forming apparatus as claimed in claim [35]36, wherein said clock phase control circuit comprises:

a high-frequency clock generator;

a first frequency divider which generates said output pixel clock by dividing an output of said high-frequency clock generator, the first frequency divider having a circuit which can change a phase of said output pixel clock;

a phase change circuit which changes a phase of said first frequency divider; and

a second frequency divider which generates an internal clock by dividing an output of said high-frequency clock generator, the second frequency divider having a circuit which can change a phase of said internal clock.

[37]38. (Amended) The image forming apparatus as claimed in claim 26, wherein said high-frequency clock generator is constituted by a PLL circuit comprising: a voltage controlled oscillator circuit; a programmable counter which divides an output of said voltage controlled oscillator circuit; and a phase comparator circuit which compares phases of an output of said programmable counter and a reference frequency, wherein said first frequency divider generates said output pixel clock by dividing an output of said voltage controlled oscillator circuit and a phase of said output pixel clock is synchronized with a phase synchronous signal.

[38]39. (Amended) The image forming apparatus as claimed in claim [37]38, further comprising a modulation pattern generating circuit which generates a modulation pattern by which an optimum exposure energy is obtained based on the image data in synchronization with said output pixel clock.

[39]40. (Amended) The image forming apparatus as claimed in claim [38]39, wherein said modulation pattern generating circuit can change a phase of the output pixel clock for each of a plurality of lines.

[40]41. (Amended) The image forming apparatus as claimed in claim [39]40, wherein said first frequency divider, said phase change circuit, said PLL circuit and said modulation pattern generating circuit are formed in a single integrated circuit.

[41]42. (Amended) The image forming apparatus as claimed in claim [40]41, wherein said integrated circuit further comprises a semiconductor laser modulation drive circuit.

[42]43. (Amended) An image forming apparatus comprising:

an optical scanning unit which scans a plurality of light fluxes on a medium to be scanned by deflecting the light fluxes by a deflector, the light fluxes being synchronous with

an output pixel clock and being modulated in accordance with image data of a respective one of a plurality of lines; and

clock phase control means for controlling a phase of said output pixel clock for each of a plurality of deflecting surfaces of said deflector so as to correct a fluctuation in a scanning length corresponding to the plurality of deflecting surfaces.

[43]44. (Amended) The image forming apparatus as claimed in claim [42]43, wherein said clock phase control means comprises:

high-frequency clock generator means;

first frequency dividing means for generating said output pixel clock by dividing an output of said high-frequency clock generator means, the first frequency dividing means having means for changing a phase of said output pixel clock;

phase change means for changing a phase of said first frequency dividing means; and

second frequency dividing means for generating an internal clock by dividing an output of said high-frequency clock generator means, the second frequency dividing means having means for changing a phase of said internal clock.